



FIG. 2
 PRIOR ART

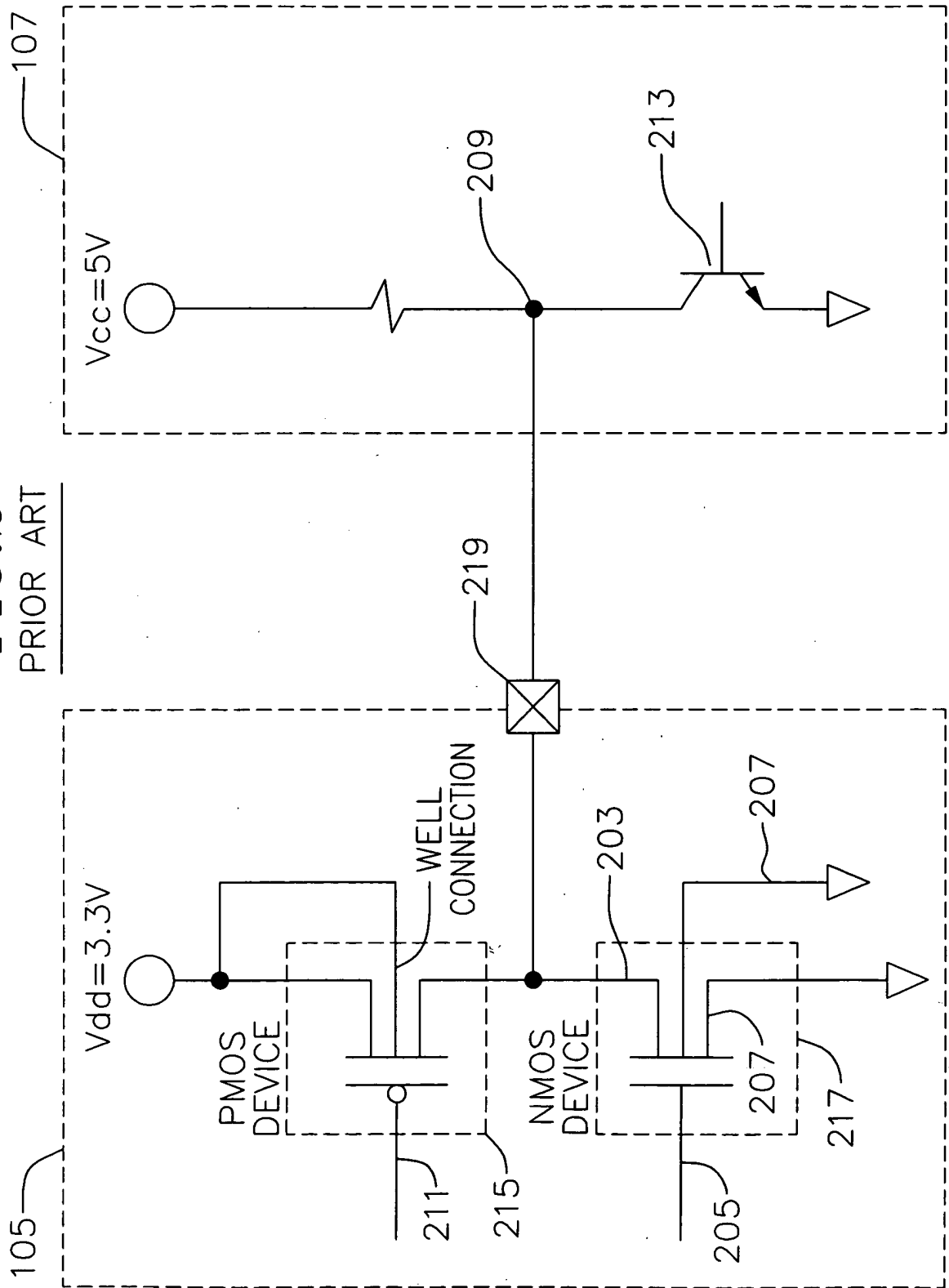
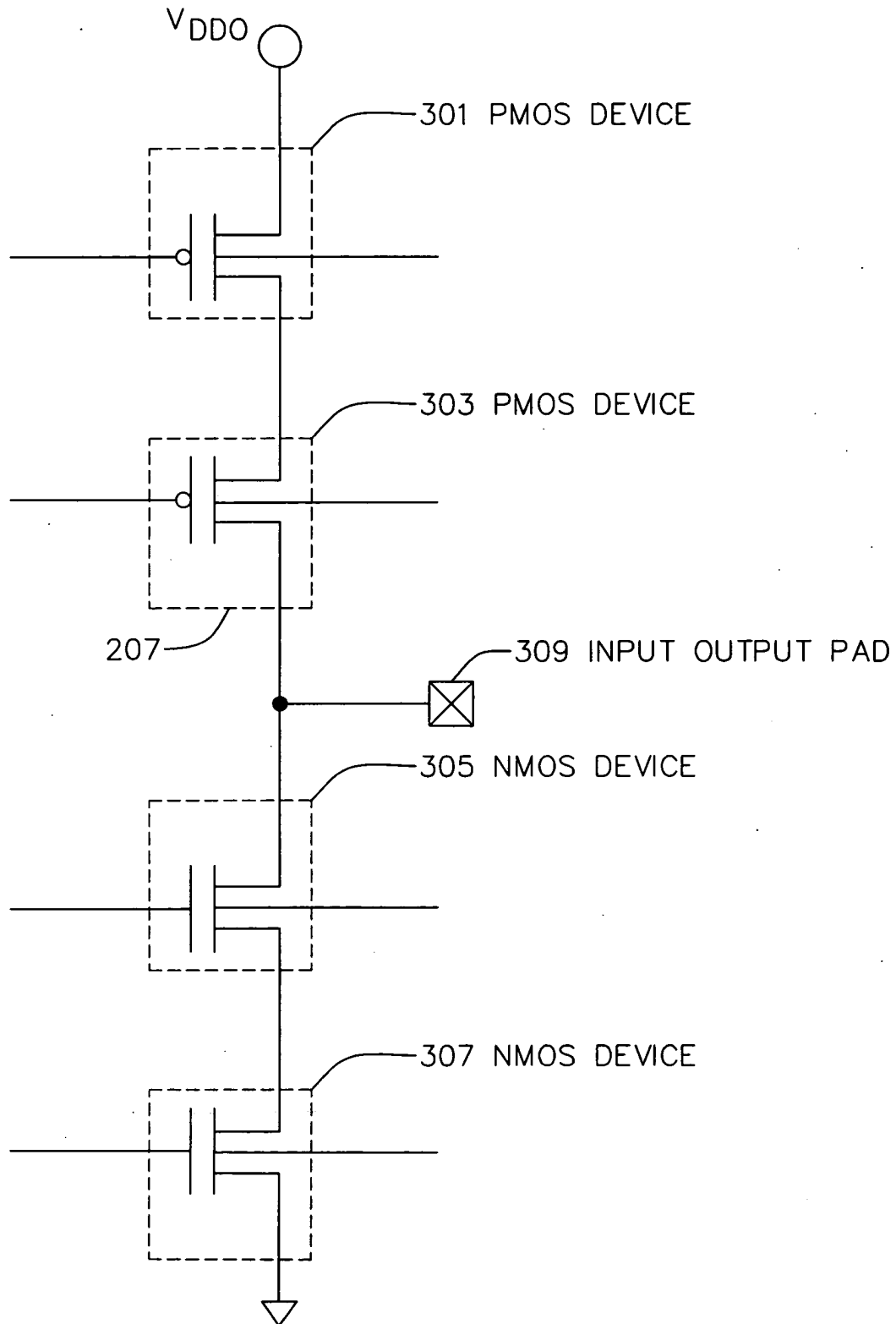




FIG. 3



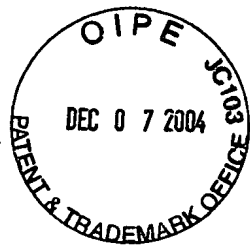
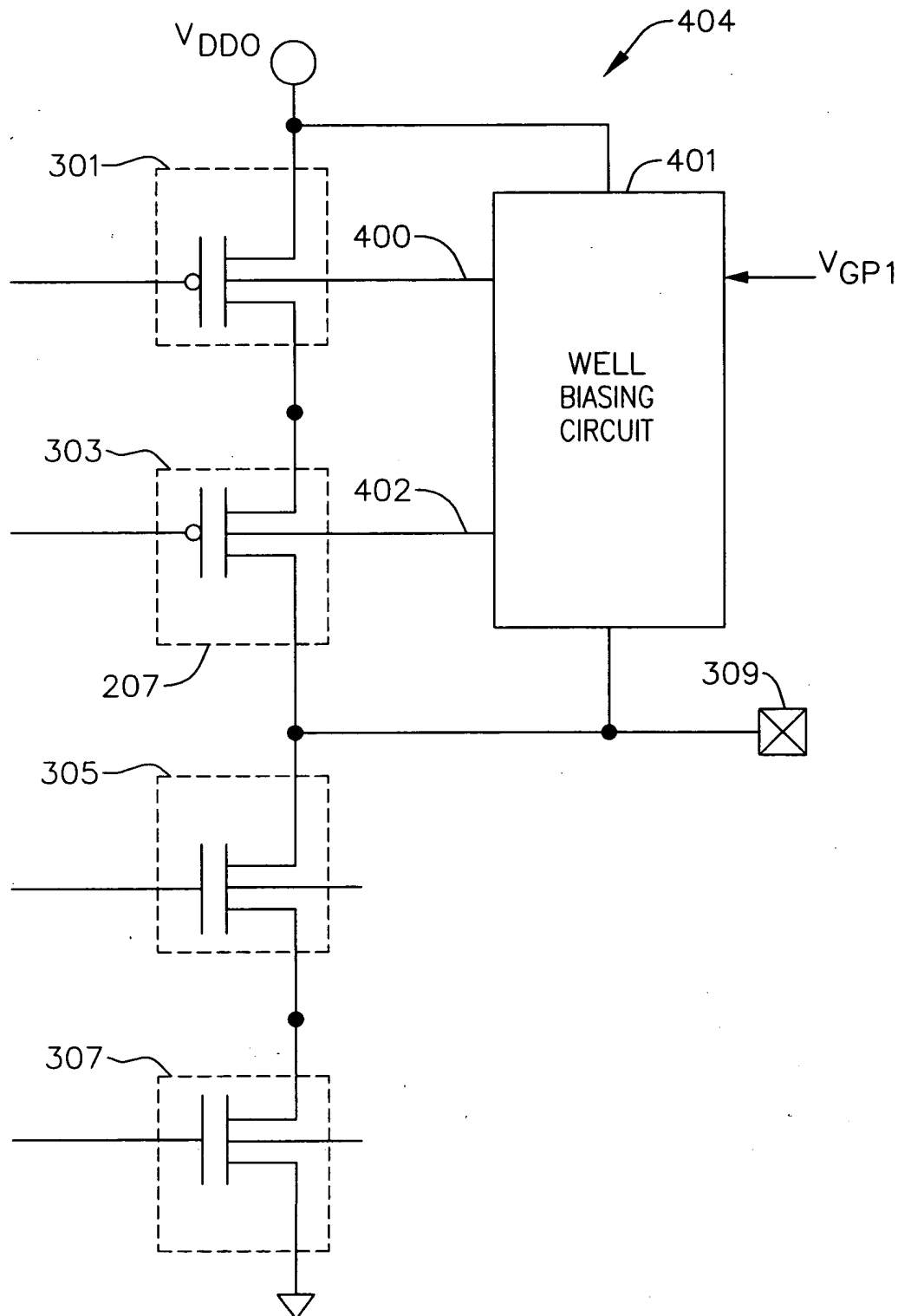


FIG. 4



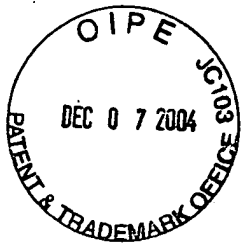


FIG.5

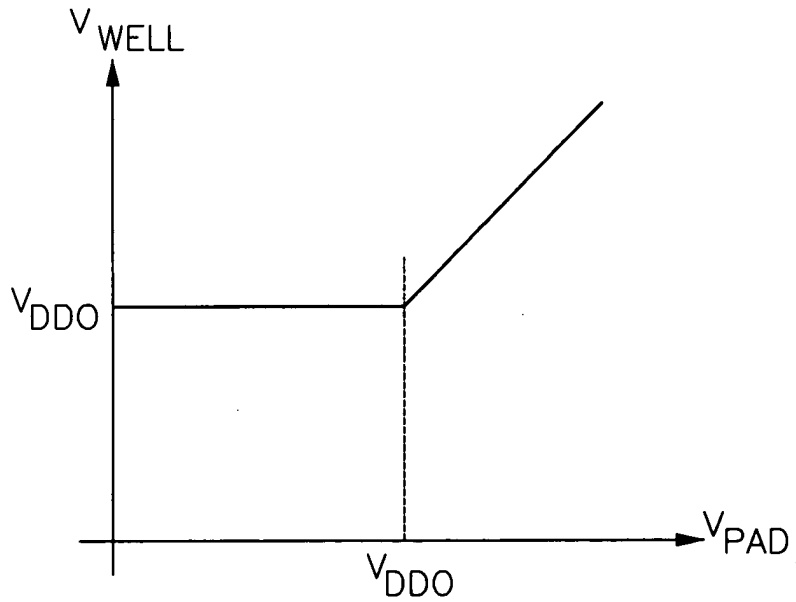




FIG. 6

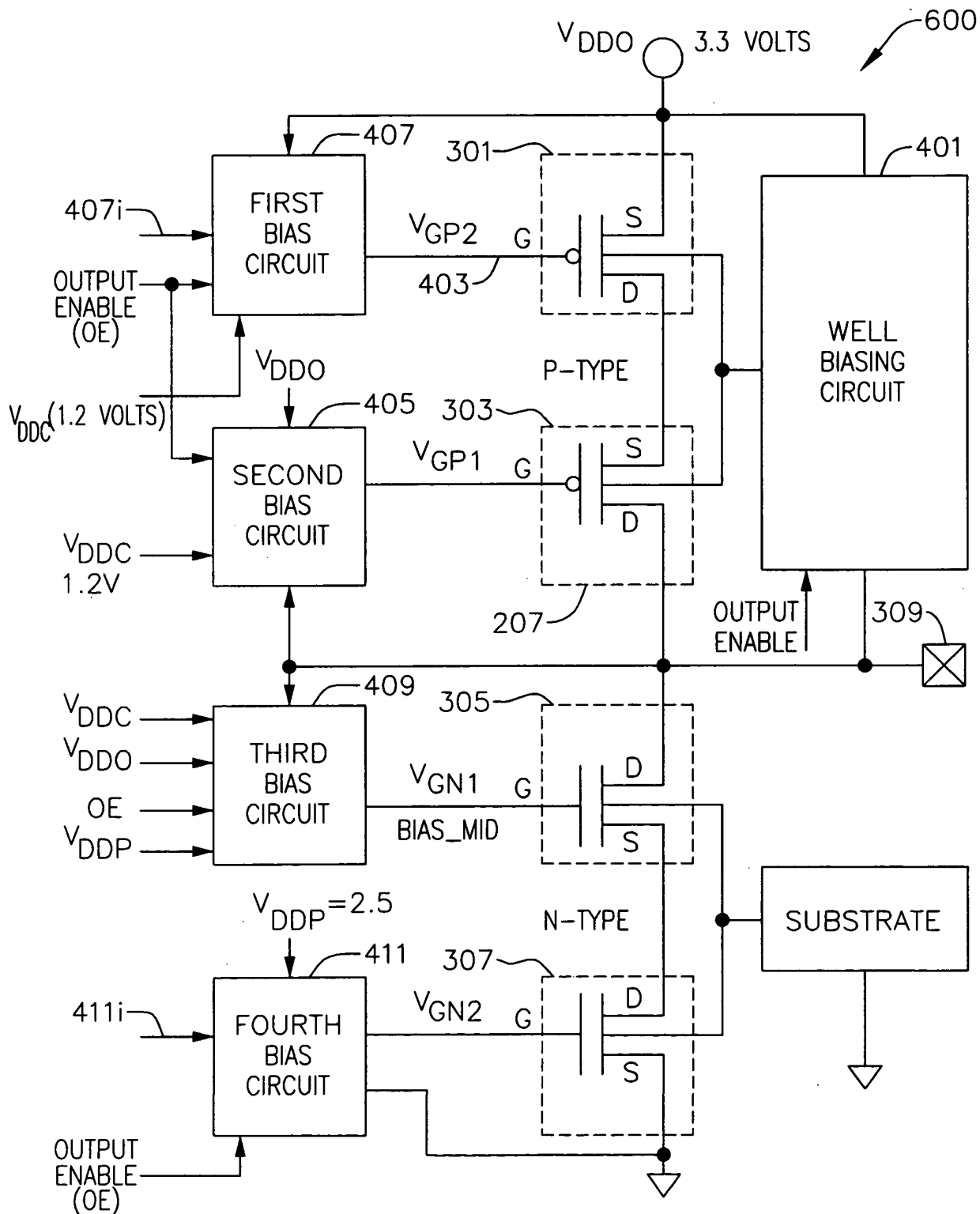




FIG. 7

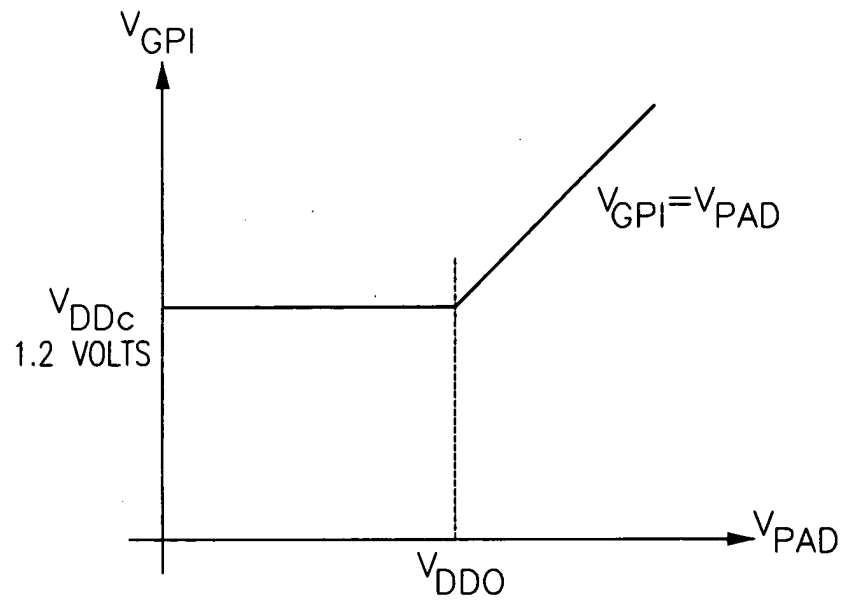




FIG. 8

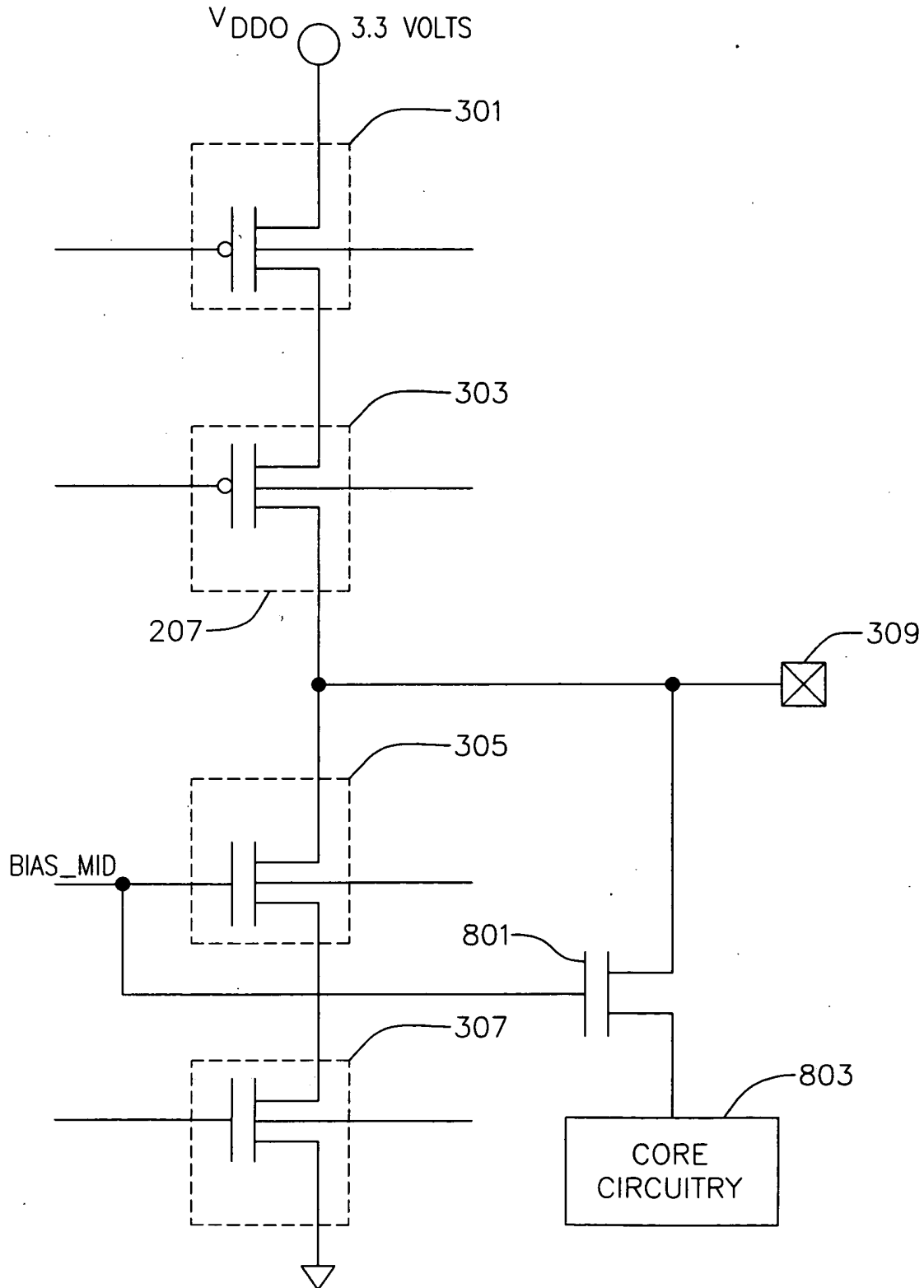




FIG. 9A

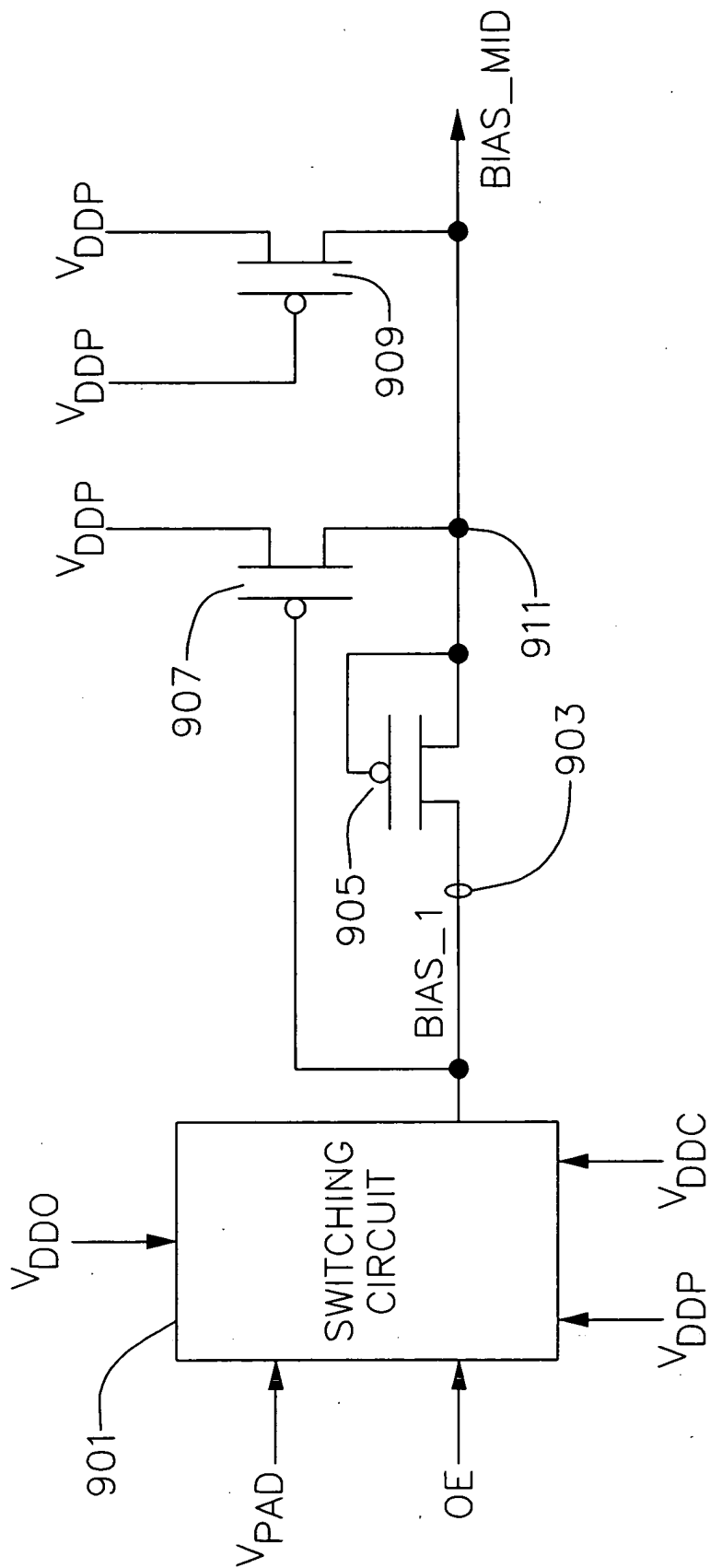
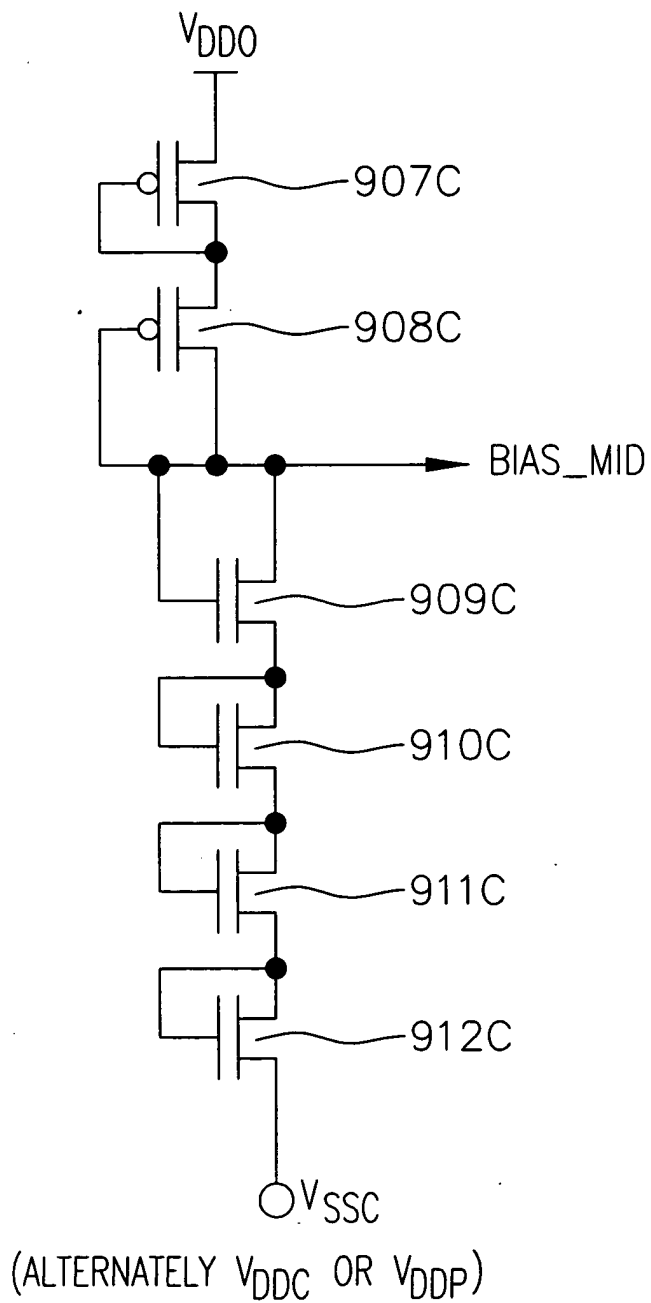




FIG. 9B



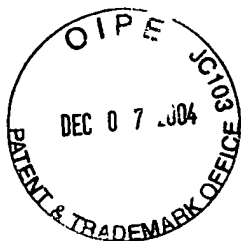


FIG. 10

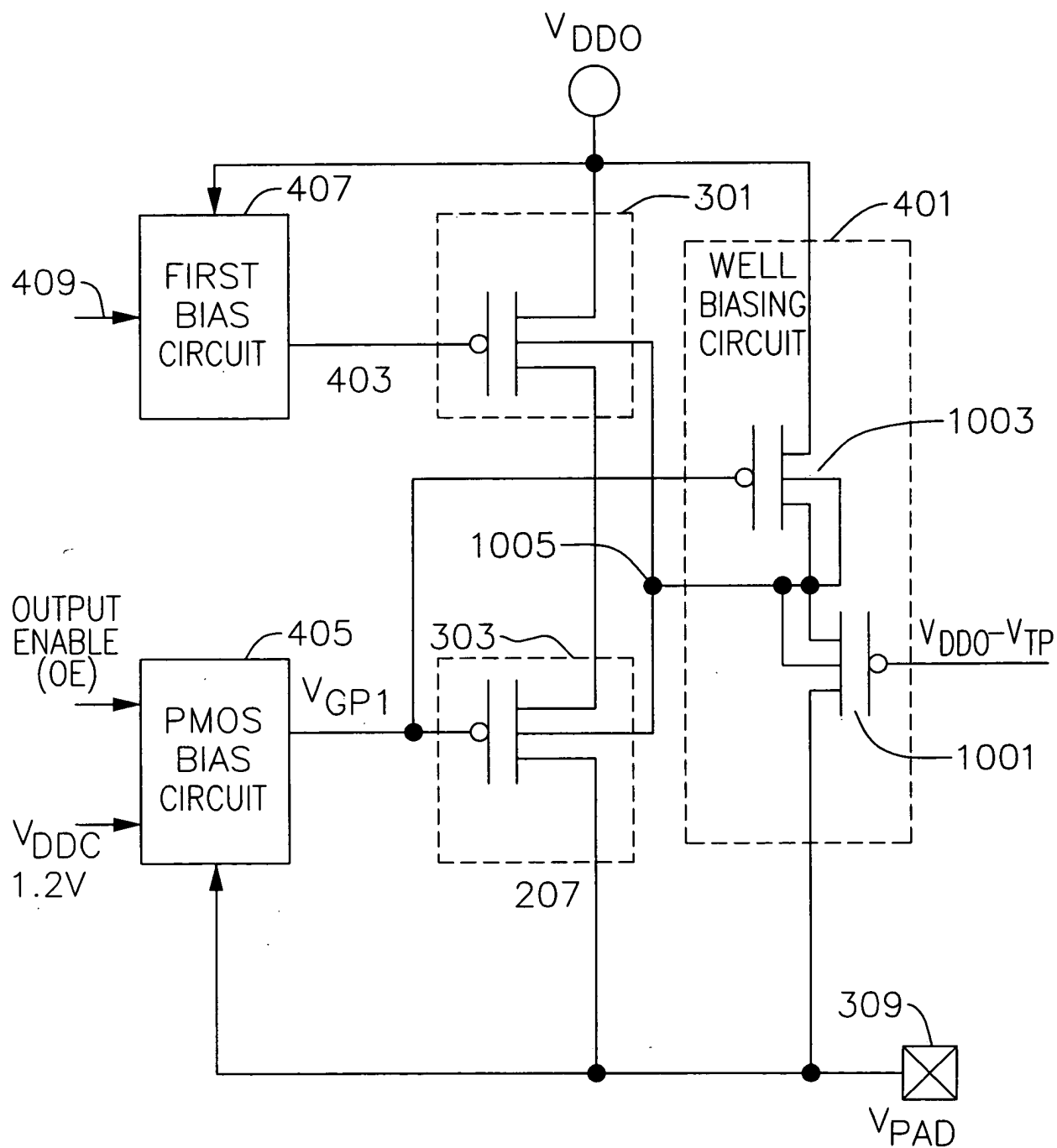




FIG. 11A

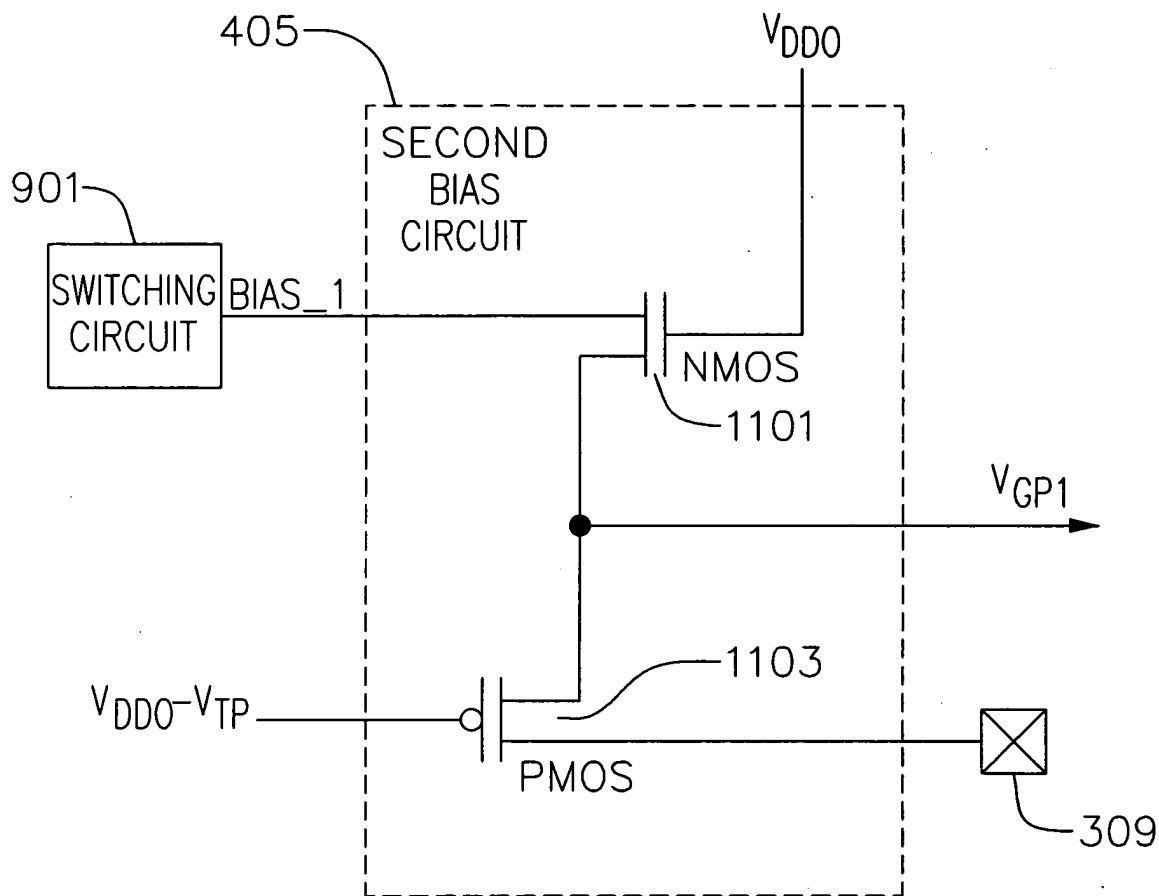




FIG. 11B

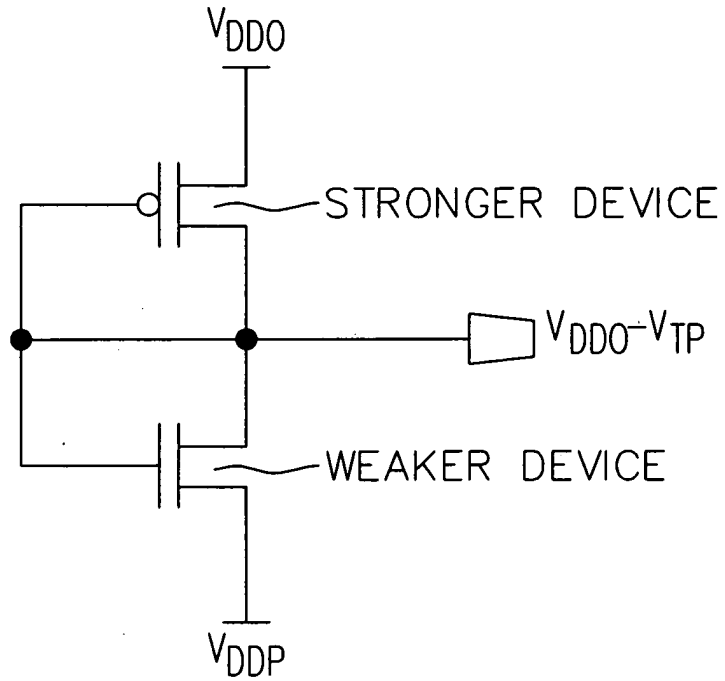




FIG. 11C

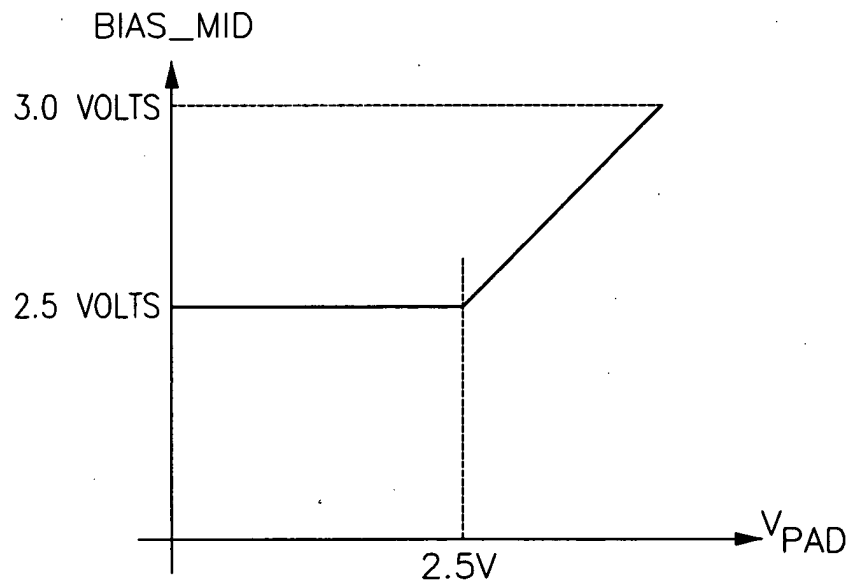
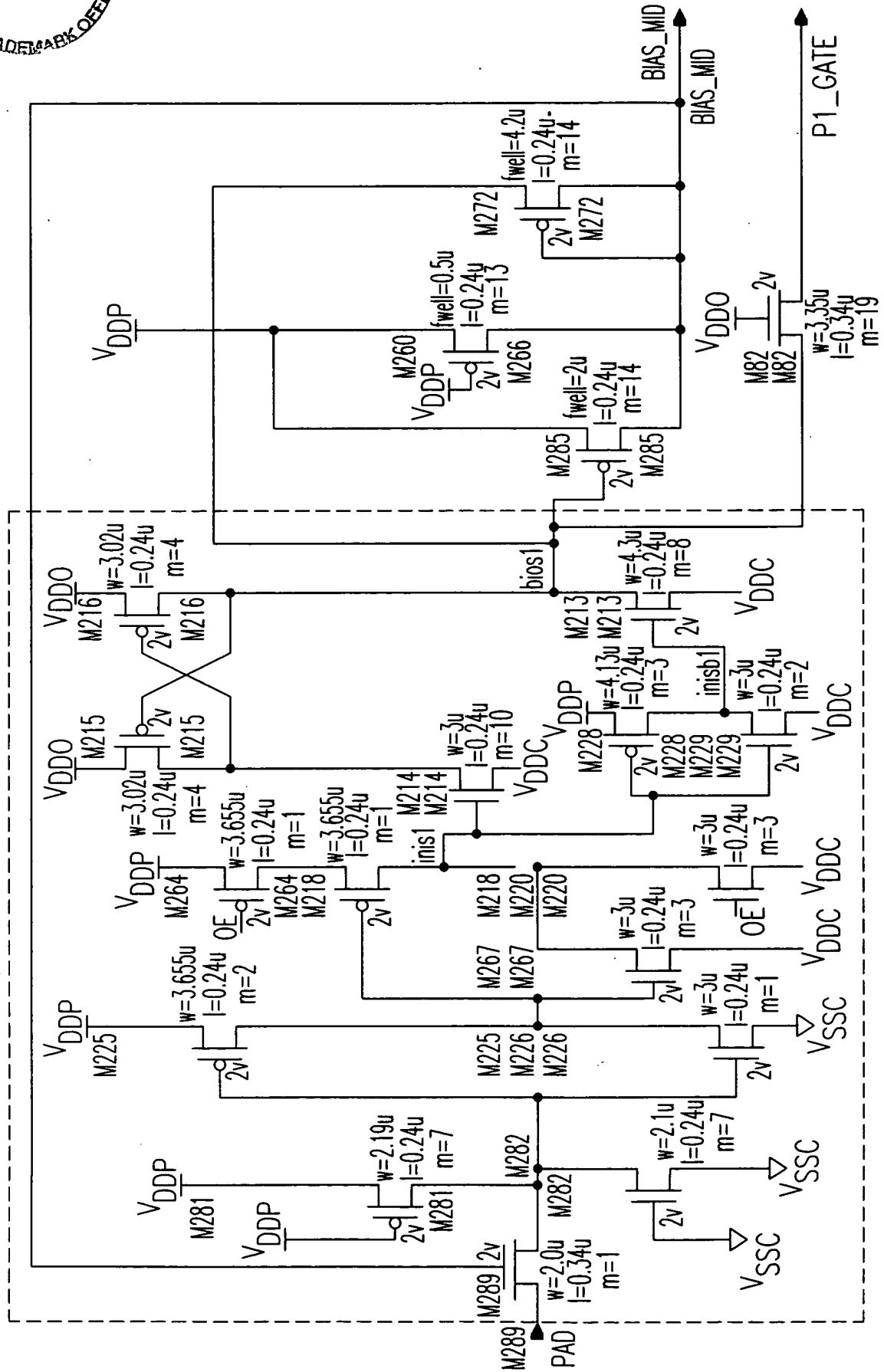




FIG. 11D

901



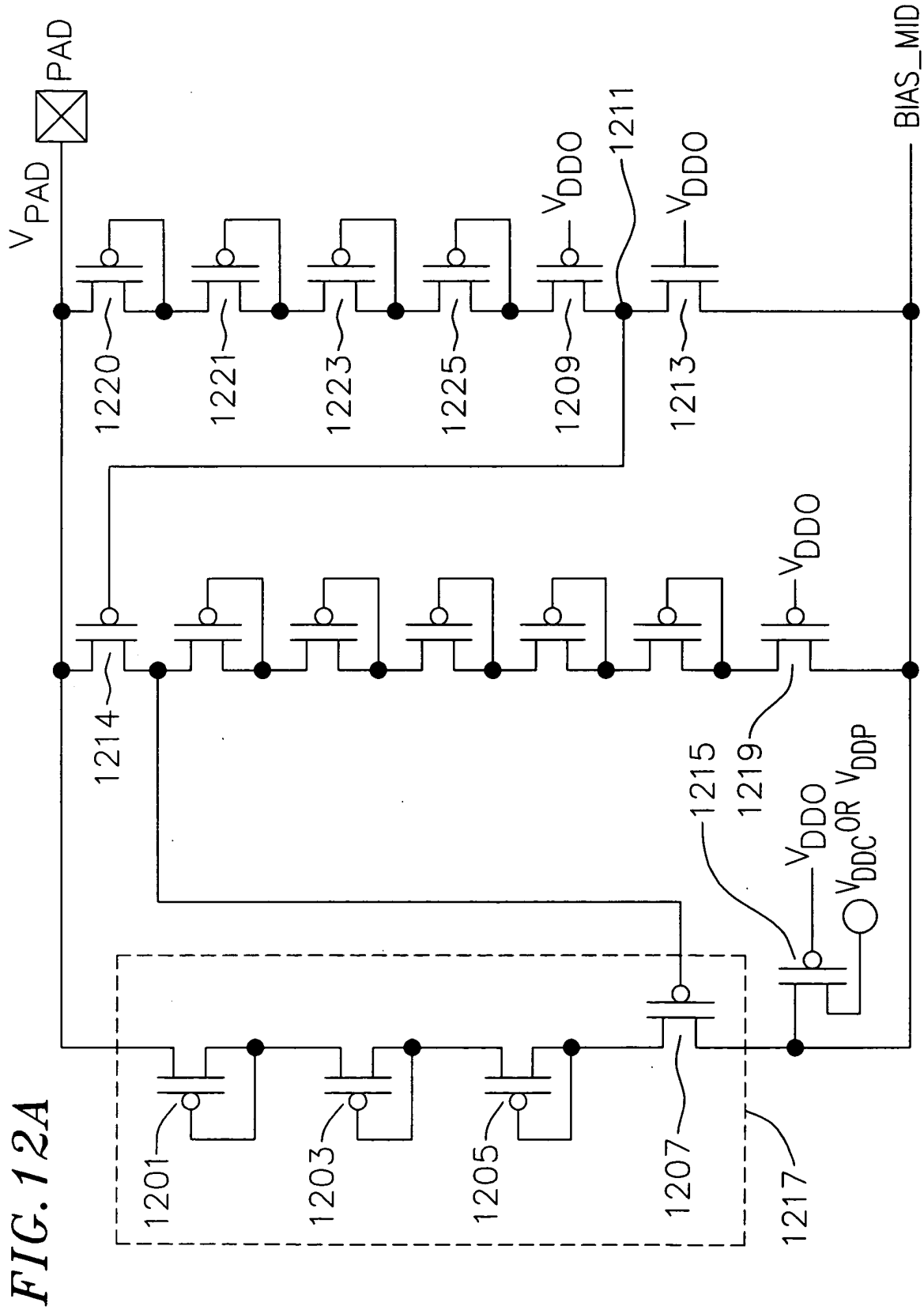




FIG. 12B

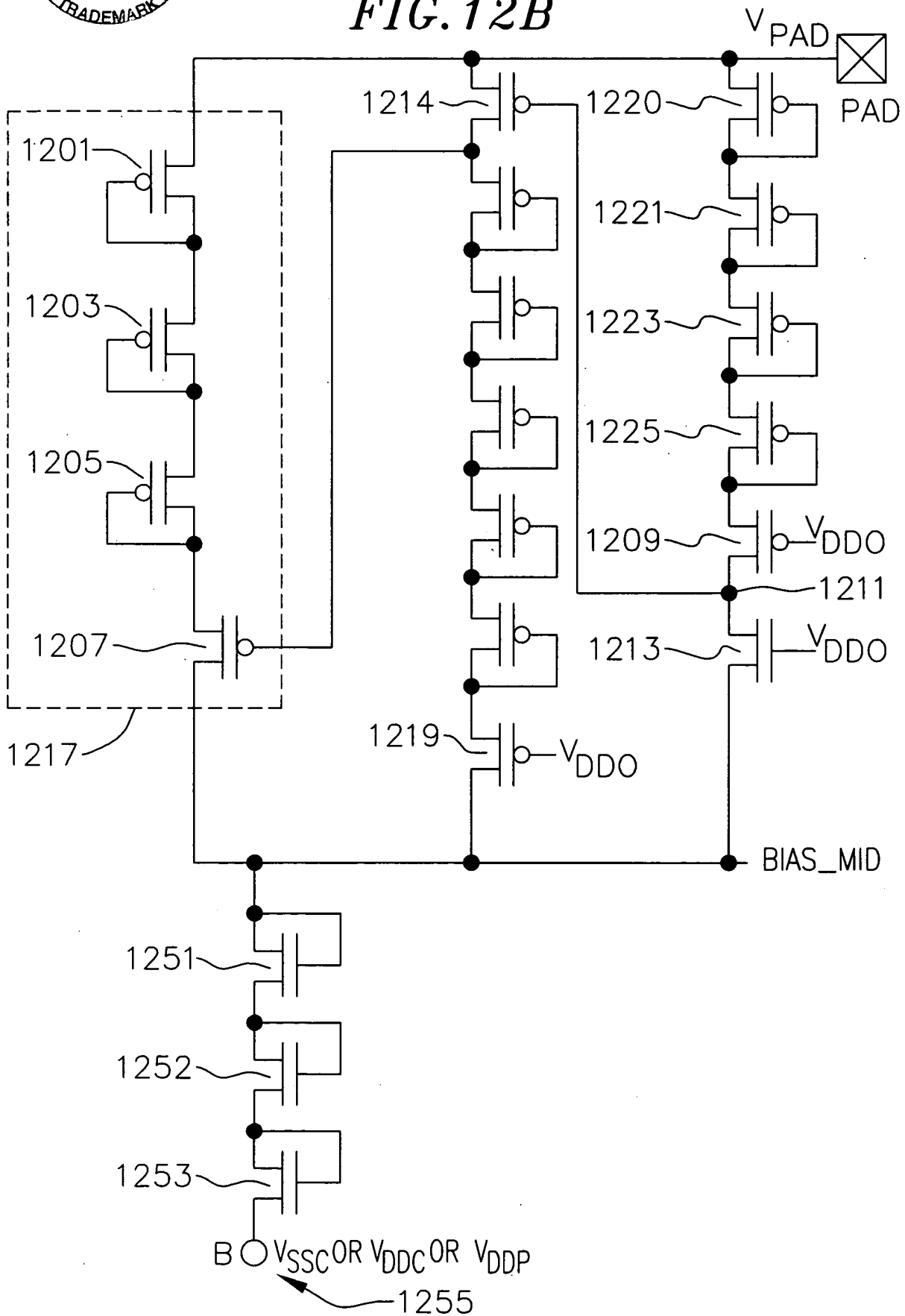




FIG. 13

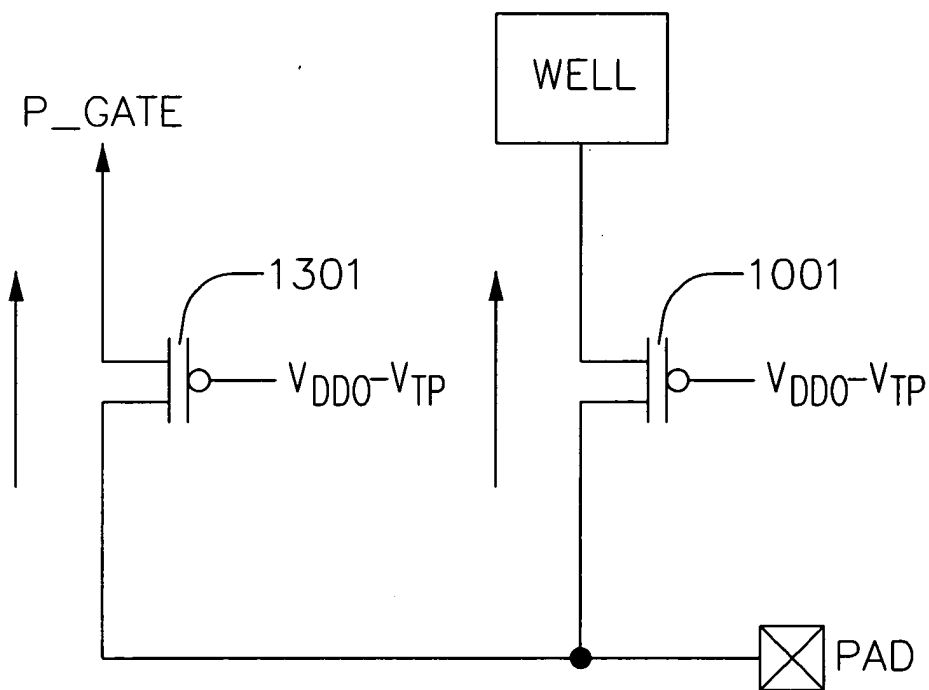


FIG. 14

The diagram illustrates a biasing system. A SWITCHING CIRCUIT (901) is controlled by V_{DDO} , V_{DDP} , V_{PAD} , and OE . Its output (903) is connected to a node that branches into two paths: one through a transistor (905) to a BIAS_1 node, and another through a transistor (907) to a node (911). This node (911) is also connected to a COUPLING SWITCH (1401) which receives V_{DDO} , BIAS_MID, and V_{DDC} signals. The output of the coupling switch (V_{PWR}) is connected to a transistor (909) which is controlled by V_{DDP} . The output of transistor 909 is connected to the BIAS_MID output line.



FIG. 15

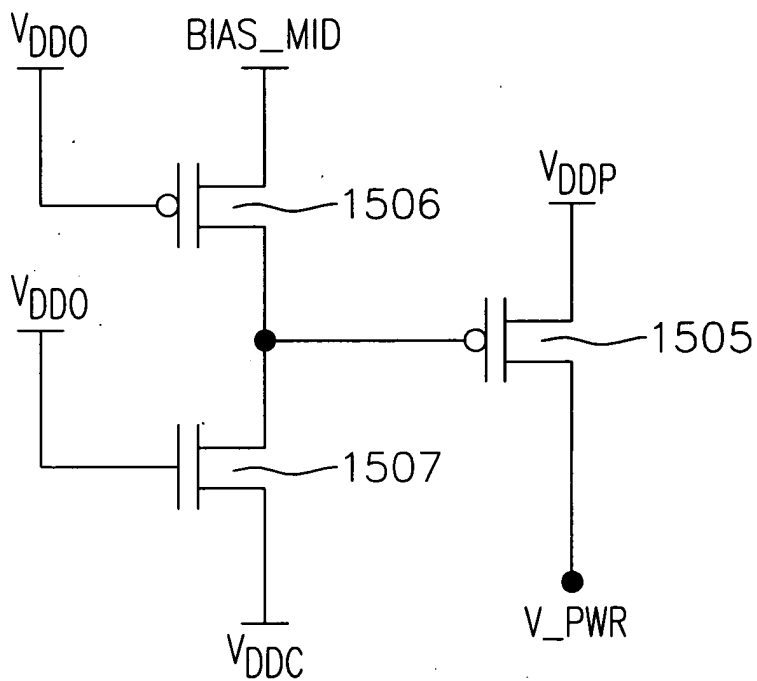




FIG. 16

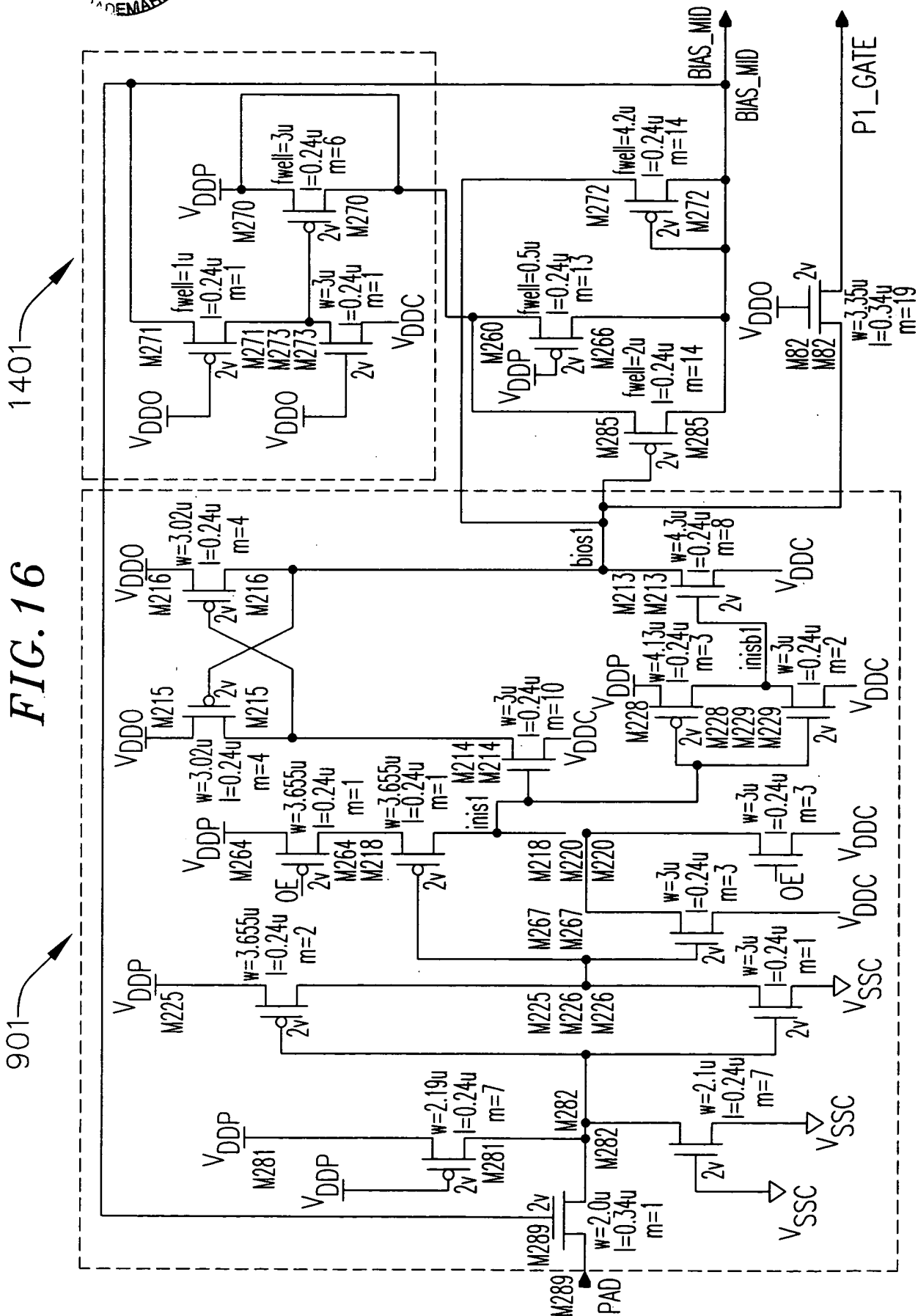
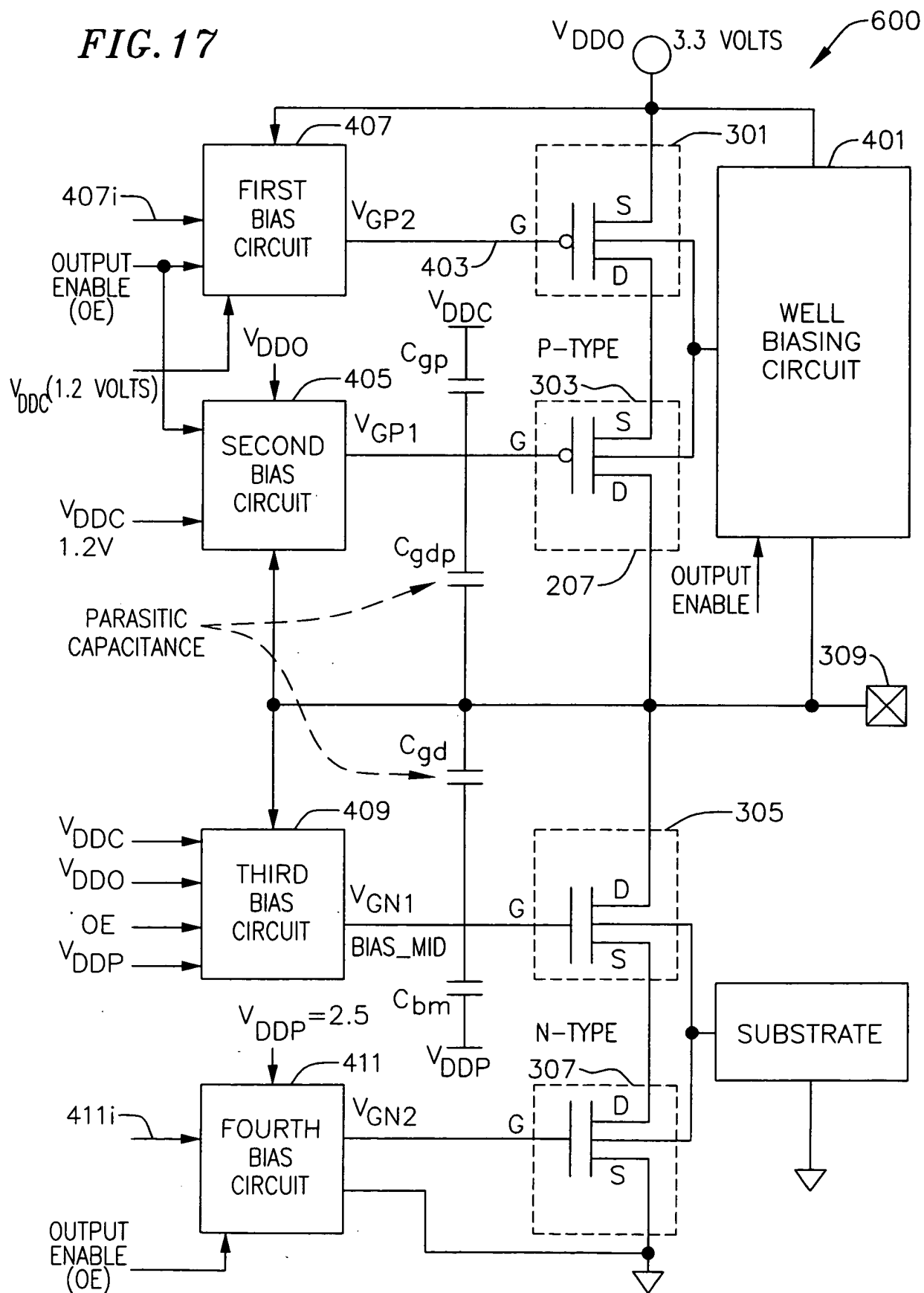
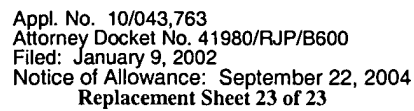




FIG. 17



[illegible]